US Sensor Efforts for ITk

Presentation Date: July 7, 2015

Chris Kenney

U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

Inner Pixels

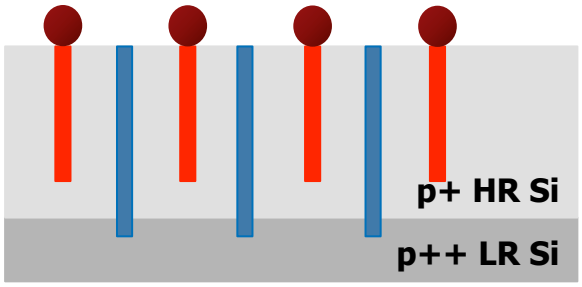
SLAC

- Due to radiation damage viable options appear to be limited to 3D diode sensors or CMOS sensors bonded to a front-end ASIC
- Suitable CMOS sensors for the inner pixels are being actively pursued in Europe, but not in the US
- 3D diode sensors are being worked on at SLAC (Stonybrook) well integrated with the global community
- Scope is at the prototype level
- Technology will be transferred to foundries

Inner Pixels – 3D Issues and Plans

SLAC

- Back side contacts for ease of assembly
- Thin sensors
  - Reduce occupancy at high eta
  - Maintain active fill factor going to smaller pixels
  - Reduce mass
  - Mechanical robustness
- 3D-diode sensors are being worked on by SLAC
  - Thin sensors < 150 microns
  - Use of bias wafer
  - Variable depths
- Sally and Martin at UNM collaborate on testing



FBK & Trento

Inner Pixels – Plans

SLAC

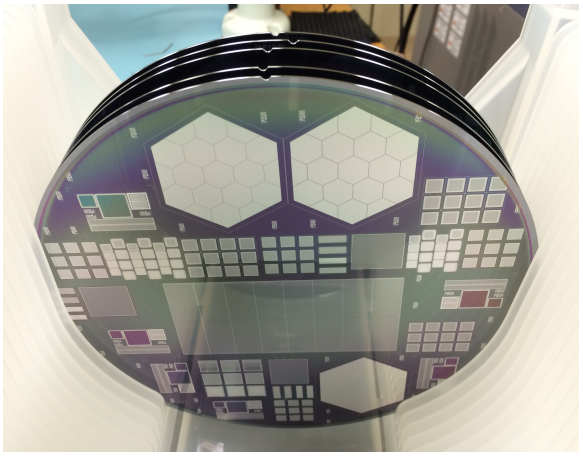
- Production of thin 3D wafers underway
  - FE-I4, RD53-1, RD53-2, etc.
  - Thicknesses of 75 μm, 125 μm, and 175 μm
- Intend to bump bond at SLAC
- Production manufacturing by proven foundries: CNM, FBK, SINTEF, etc.

- Biggest challenge may be full-scale production

Mid Pixels

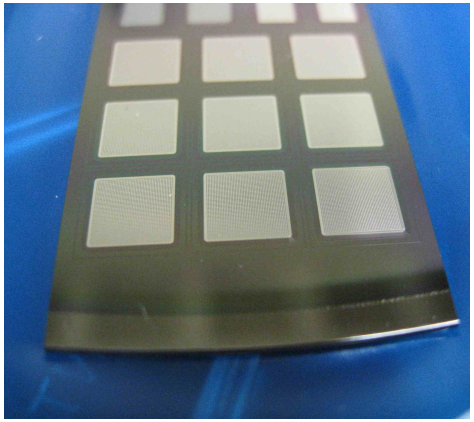
SLAC

- Hybrid with planar sensors bonded to FE-IC
- Thin run is underway at SLAC
  - 75 μm thick
  - Matched to FE-I4, RD53



200-mm FZ wafers!

- Novati
  - Led by FNAL
  - Establish a US sensor vendor for HEP
  - SLAC (J. Segal) contributed the sensor fabrication process
  - First batch done and works ok
  - 200 mm wafers



Outer Pixels

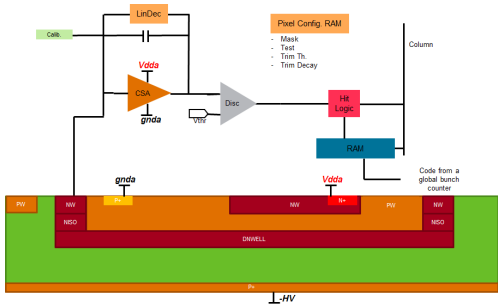
SLAC

- Either hybrid design similar to IBL or Monolithic CMOS Sensors

- US is actively pursuing Monolithic CMOS Sensors
- 6th and possibly 5th layers targeted
- **Cost is the driver**
- Institutions involved: SLAC, LBNL, Bonn
- “COOL” chip is under design (CmOs for Outer Layers)
- Involves integrated circuit and sensor design
- Will need extensive help in the testing of the prototype parts
- Irradiations and testing with UNM

Outer Pixels

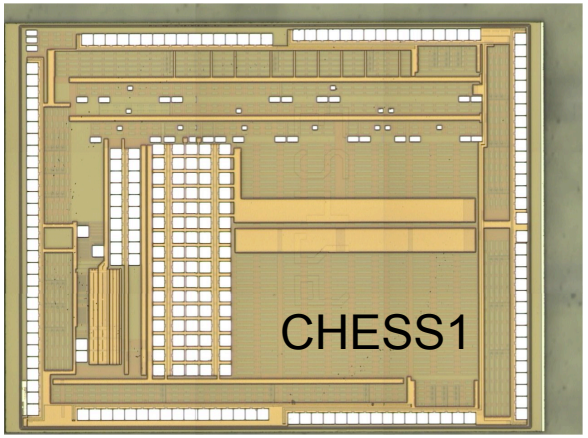
- Challenges
  - Signal charge collection
  - Radiation tolerance
  - Fitting complex circuitry inside 50 x 250 μm^2 pixel
  - **Short time scale**
- COOL 1 expect to submit in the fall
  - Using LFoundry as fabrication partner
  - Full-wafer run, multiple substrate resistivities
  - Second COOL 2 submission in early 2016
- LBNL working with Semiconductor Creations via SBIR
  - Using ON Semiconductor as fabrication partner
-



Strips

SLAC

- Options are diode arrays wire bonded to front-end ASICs or CMOS sensors
- Very aggressive program to demonstrate suitability of CMOS sensors in US (also in UK)
- Would reduce system costs
- Improve spatial resolution
- Main challenges:
  - **Short time frame**
  - Radiation tolerance
  - Signal collection
- Central team working on design of the CMOS sensors is UCSC, SLAC, and KIT
- Large global effort involved in testing of prototypes



Strips

SLAC

- CHESS1 chip submitted in fall, 2014
  - Extensively tested
- CHESS2 under design
  - Full-wafer run
  - Multiple substrate resistivities
  - Implements full functionality in reduced area
  - Submission expected late summer, 2015
  - Testing and irradiation campaign – can't have too much help

Production

SLAC

Strip CMOS sensors

AMS has capacity of 160,000 200mm wafers per annum

ATLAS needs on the order of 10% of this

So need maybe 2 months of the fab over a 18 month period

Pixel CMOS Sensors

LFoundry states a capacity of 40,000 200mm wafers per month

ATLAS would need on the order of 500 wafers per outer layer

So a few days worth of capacity …

Quality control and assembly will dominate the construction time

Production

SLAC

- For CMOS options
- Develop testing procedure
- Partner with local company to identify KGD at wafer level

- For diode array sensors – transfer to industry
- Help with quality monitoring

Deliverables

- 3D and Thin Planar Sensors
  - Prototype parts distributed for testing
  - Establish process for foundaries
  - Bump bond to relevant ASICs
- CMOS Strips and Pixels
  - Functional Integrated circuit design
  - Established radiation tolerance
  - Parts for beam tests

- If selected US should
  - Act as interface to foundries
  - Lead wafer-level testing and singulation
  - Play significant role at module level